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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,767	10/12/2005	Jeroen Anton John Leijten	260692	2219

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
12/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,767	LEIJTEN, JEROEN ANTON JOHN	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 and 5-13 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE and Amendment as received on 9/17/2008.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-6, and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., U.S. Patent No. 5,748,936 (herein referred to as Karp), in view of Kogge, "The Microprogramming of Pipelined Processors," 1981 (herein referred to as Kogge).

5. Referring to claim 1, Karp has taught a processor arranged for execution of a program, the processor comprising:

a) a plurality of execution units, comprising at least a first execution unit and a second execution unit. See Fig,2, components 30.

b) a register file accessible by the execution units. See Fig.2, components 32, and column 5, lines 7-8. Note that one register file may exist, or multiple register files may exist, where in the case of multiple register files, each would be a sub-file making up an overall register file.

c) a communication network for coupling the execution units and the register file. See Fig.2. Clearly, execution units must be coupled to the register file(s).

d) a controller arranged for controlling the processor based on control information derived from the program, characterized in that at least the first execution unit and the second execution unit are arranged to produce, according to a programmed criterion, a second identifier on validity of an output result for corresponding output ports of the first and second execution units, the processor being arranged to dynamically control writing of result data corresponding to an operation into the register file, based at least on the second identifier. See Fig.5 and column 10, lines 1-60. Note that result writing is based on predicate, poison bit, and exception information. At least one of these items qualifies as the second identifier. For instance, the second identifier may be considered the poison bit, which is set based on whether an exception was generated (result invalid) or not generated (result valid). It should be further noted that the setting of the bit is performed according to a programmed criterion. That is, everything a processor does is according to some programmed criterion. In this case, the processor is programmed to write a particular value in a poison bit according to detection of an exception/error. For example, the processor is able to detect that a floating-point exception occurs, and that a poison bit should be set in response to such an exception, because the system has been programmed to look for floating-point errors (column 10, lines 43-45).

e) Karp has taught a data-stationary processor but has not taught a time-stationary processor, as known in the art. However, Kogge has taught the concepts of both data-stationary and time-stationary control. More importantly, Kogge has taught that a pipeline can support both types of controls. See the 1st full paragraph on page 65. The implementation of time-stationary control

requires the hardware of Fig.2(a) and the implementation of data-stationary control requires the hardware of Fig.2(b). Hence, it can be seen that implementing time-stationary control requires fewer buffers (less hardware) than its counterpart. Consequently, it would have been obvious to one of ordinary skill in the art to modify Karp to include time-stationary control as opposed to data-stationary control. One would be motivated to make such a combination to reduce hardware cost, and further, the producing an identifier on validity of a result would still apply because time-stationary processors are able to support conditional branches. See page 67, column 2, and page 68. The validity identifier in Karp is produced in response to branch instructions when speculative execution begins.

6. Referring to claim 2, Karp in view of Kogge has taught the processor according to claim 1, characterized in that the control information further comprises a first identifier on the validity of the operation, and wherein the processor is arranged to dynamically control writing of result data corresponding to the operation into the register file, based on the first identifier and the second identifier. See Fig.5 and column 10, lines 1-21. Note that the first identifier may be interpreted as the predicate information. Essentially, at any point before results are to be written, if it is determined that a predicate is false and that an instruction should not modify the state of the system, result data is not written to the register file. If the predicate is true, then result data could be written to the register file if other factors are satisfied. The other factors include the poison bit value and whether an exception was generated. Either one of these qualify as the second identifier. For instance, see Fig.5, step 212, and column 10, lines 58-60. Note that the second identifier (an exception identifier) identifies whether an exception has occurred for a

given instruction, i.e., whether that instruction has erred in some manner. If an exception occurs, then results are not written. Results are written if an exception does not occur.

7. Referring to claim 3, Karp in view of Kogge has taught the processor according to claim 2, characterized in that the first identifier is delayed according to the pipeline of the corresponding execution unit arranged for executing the operation. See column 10, lines 16-21.

8. Referring to claim 5, Karp in view of Kogge has taught the processor according to claim 3, characterized in that the processor is further arranged to dynamically control writing of result data corresponding to the operation into the register file, based on the first identifier, the second identifier and an input datum. See Fig.5, and note that each of the first identifier (predicate), the second identifier (exception), and an input datum (either poison bit shown in Fig.5, step 208, or the result itself, which is an input to the register file) plays a role in controlling writing to the register file.

9. Referring to claim 6, Karp in view of Kogge has taught the processor according to claim 1, characterized in that the register file is a distributed register file. See Fig.2 and note that a register file is divided into multiple sub-register files 32) which are distributed throughout the system for use by the execution units.

10. Referring to claims 8-12, claims 8-12 are rejected for the same reasons set forth in the rejections of claims 1-3 and 5-6 above, respectively.

11. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp in view of Kogge and further in view of the examiner's taking of Official Notice.

12. Referring to claim 7, Karp in view of Kogge has taught the processor according to claim 1. Karp has not explicitly taught that the communication network is a partially connected communication network. However, Official Notice is taken that partially connected communication networks, and their advantages, are well known and accepted in the art. A partial network is where at least one execution unit is coupled to less than N register files. One example would be where integer circuitry is couple to an integer register file and floating-point circuitry is connected to a floating-point register file. Since, integer circuitry does not operate of floating-point numbers or write floating-point numbers, then the integer unit does not have to be coupled to the floating-point register file. Clearly, by requiring less wiring than a fully connected network, the partial network is less expensive in terms of silicon. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Karp such that the communication network is a partially connected communication network.

13. Referring to claim 13, claim 13 is rejected for the same reasons set forth in the rejection of claim 7 above.

Response to Arguments

14. Applicant's arguments filed on September 17, 2008, have been fully considered but they are not persuasive.

15. Applicant argues the novelty/rejection of claim 1 on page 7 of the remarks, in substance that:

> "Applicant's claimed "second identifier" differs from the "exceptions" and "poison bit" described in Karp and referenced in the Office Action's rejection of independent claims 1 and 8. Karp's disclosed poison bit value merely indicates whether earlier in an instruction stream an exception was generated. See, Karp, Figure 5, blocks 212, 214. The poison bit, resulting from the generation of an exception, cannot be used for Applicant's claimed custom operation - in

> particular Applicant's recited "dynamically control writing of result data corresponding to an operation into the register file.'
>
> In a processor incorporating Applicant's claimed invention, a programmer dictates, via a programmable criterion, conditions under which a valid operation has occurred. In the processor disclosed in Karp, there is a fixed/predetermined (i.e., non-programmable) set of conditions, usually defined by the machine architecture, that result in an exception and thereafter a setting of the poison bit. This essential difference is clarified in claims 1 and 8 by specifying that the second identifier is produced according to a programmable criterion."

16. These arguments are not found persuasive for the following reasons:

a) Even if the exceptions that Karp detects are fixed/predetermined, this does not mean that they aren't programmed criterion. That is, a programmer programs the system of Karp to look for particular errors, and if they occur, poison bits are set, and writing of results is dynamically controlled.

17. Applicant argues the novelty/rejection of claim 2 on pages 7-8 of the remarks, in substance that:

> "Furthermore, Applicant submits that the invention recited in dependent claims 2 and 9 is not disclosed in the combined teachings of the cited prior art references. In the processor according to an embodiment of the present invention, an unnecessarily large code-size is avoided by indicating the absence of instructions, i.e. NOP operations; by single bits in a header attached to the front of the VLIW instruction. In the illustrative embodiment of the invention recited in claims 2 and 9, a first identifier is used to indicate the presence of a NOP and therewith to disable the writing back of result data. Moreover, the first identifier is delayed according to the pipeline arranged for executing the operation. By delaying the first identifier according to the pipeline of the execution unit, the information required for determining the write back of result data becomes available at the output of the execution unit at the same time as the result data itself. The latter result, incorporated into the recited elements of claims 2 and 9, is by no means disclosed by Karp. In fact, Karp points away from this measure. Karp, at col. 10, lines 16-21, states that the predicate may not be known until later because it is being computed as the current operation proceeds through the pipeline process. On the contrary, in the processor according to the present invention the first identifier is known, but it is delayed."

18. These arguments are not found persuasive for the following reasons:

a) Applicant appears to be arguing limitations that are not in the claims. Claim 2 mentions nothing about headers and NOP instructions. Furthermore, as discussed in the cited passage, the setting of the first identifier, i.e., predicate, is delayed (and hence, the predicate is delayed). The

claims say nothing about the predicate being known before delaying. In Karp, the predicate is known, but its value is simply not set until a later point in time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
November 12, 2008